Litho today, litho tomorrow

Martin van den Brink
President & Chief Technology Officer

31 October 2016

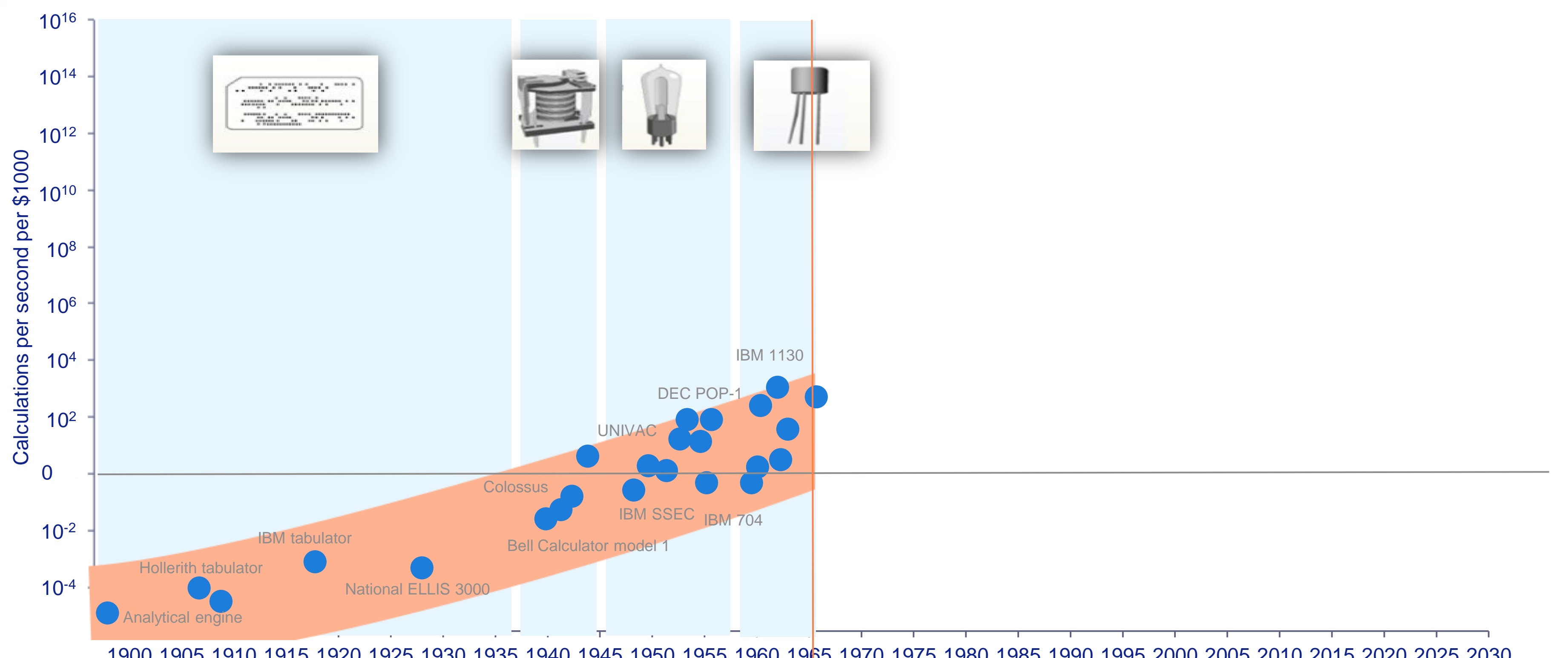
Overview

Industry trends	• Application trends and economics in our ecosystem are **driving increasing demand for processing power, high-speed memory, and low-cost storage,** fueling the continuation of **Moore's law**
Semiconductor impact	• Continuation of Moore's law will be supported by improving **patterning solutions**, achieving fast **yield ramp-up,** to realize **attractive economics**
Strategic priorities	• As a result, our strategic priorities are: **EUV industrialization, DUV competitiveness,** leadership in **Holistic lithography** and **EUV extension** with High NA
Lithography Roadmap	• We have underpinned our priorities with a **detailed product roadmap**

The world before 1965 was already on a Moore's like law

… computing speed/€ had been doubling every 2 years **for 65 years**

ASML



Moore's Law

Source: Ray Kurzweil

When ASML started Moore’s law was effective for 84 yrs

Calculations per second per $1000

10^{16}
10^{14}
10^{12}
10^{10}
10^{8}
10^{6}
10^{4}
10^{2}
0
10^{-2}
10^{-4}

Altair 8800
IBM 1130
IBM AT-80266
DEC POP-1
IBM PC
UNIVAC
Apple II
DEC POP-10
Colossus
IBM SSEC
IBM 704
IBM tabulator
Bell Calculator model 1
Hollerith tabulator
National ELLIS 3000
Analytical engine

1900 1905 1910 1915 1920 1925 1930 1935 1940 1945 1950 1955 1960 1965 1970 1975 1980 1985 1990 1995 2000 2005 2010 2015 2020 2025 2030

Moore’s Law **ASML is founded**

Source: Ray Kurzweil

Today Moore's law is effective for 116 years

Calculations per second per $1000

10^{16}
10^{14}
10^{12}
10^{10}
10^{8}
10^{6}
10^{4}
10^{2}
0
10^{-2}
10^{-4}

Core i7 quad
AMD A8
Pentium G4400
Core 2 duo
Pentium IV
Core i3
Pentium III
Pentium II
Compaq Deskpro 386
Pentium
Altair 8800
IBM 1130
IBM AT-80266
DEC POP-1
IBM PC
UNIVAC
Apple II
DEC POP-10
Colossus
IBM SSEC
IBM 704
IBM tabulator
Bell Calculator model 1
Hollerith tabulator
National ELLIS 3000
Analytical engine

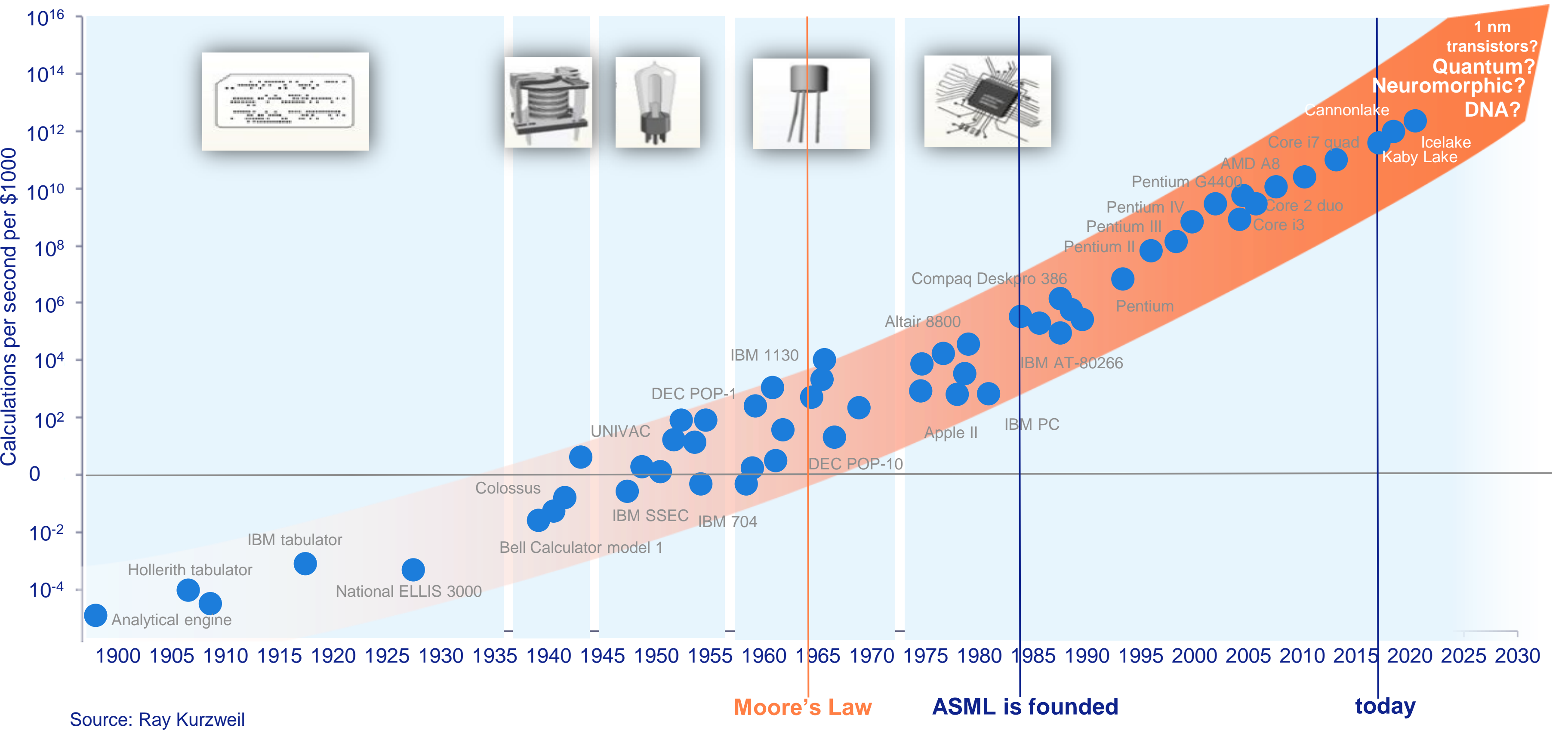
1900 1905 1910 1915 1920 1925 1930 1935 1940 1945 1950 1955 1960 1965 1970 1975 1980 1985 1990 1995 2000 2005 2010 2015 2020 2025 2030

Moore's Law **ASML is founded** **today**

Source: Ray Kurzweil

Can exponential curves continue forever?

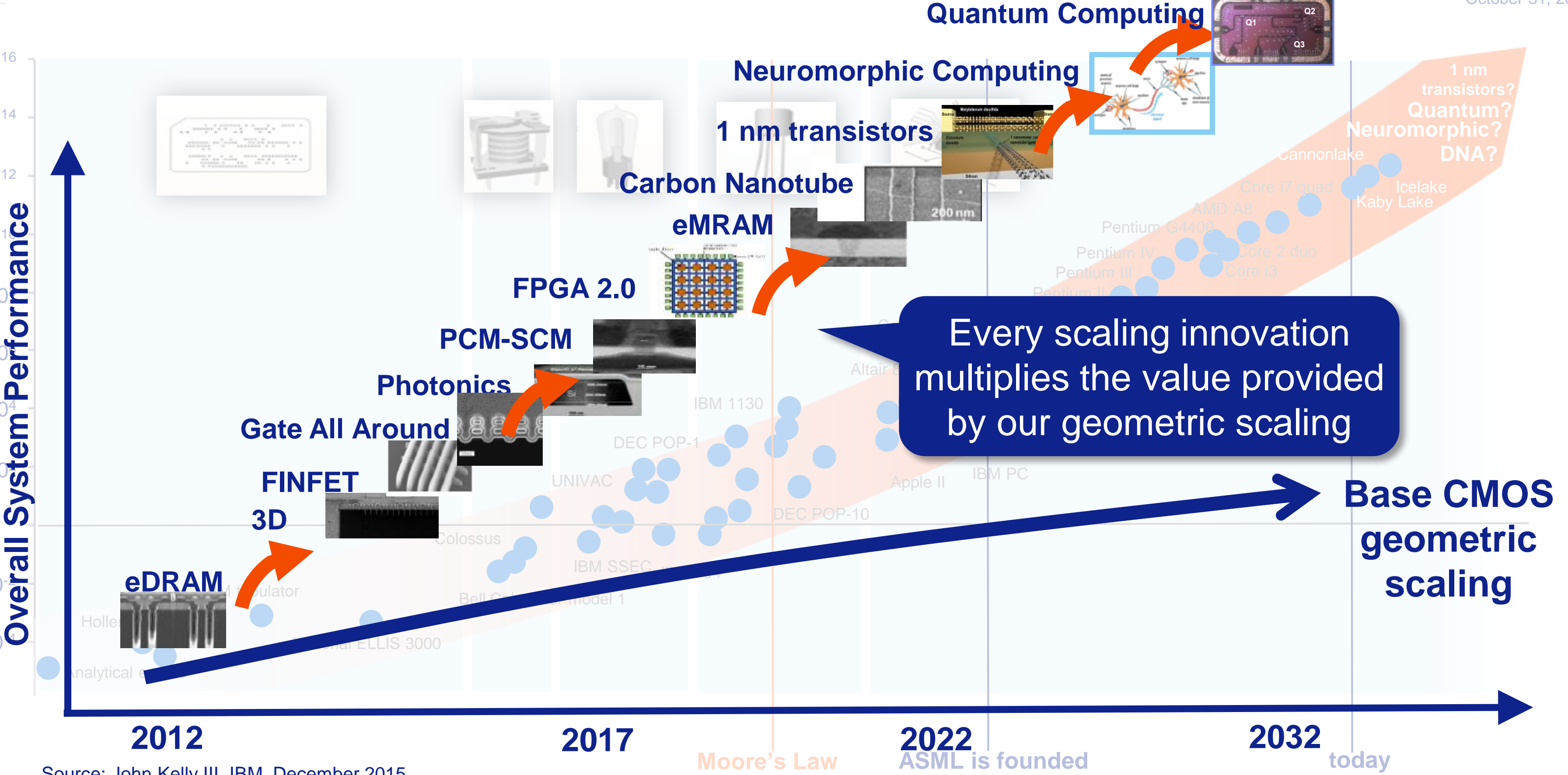
Moore's Law is likely not slowing down as long as new idea's



Source: Ray Kurzweil

Long term multi-decade device roadmap

Substantial performance gain next to the impact of geometric scaling



Source: John Kelly III, IBM, December 2015

Application trends in our industry
drive continued demand for Moore's Law

Industry trends towards 2020 and beyond

50B connected **Internet of Things** devices – needing low-cost devices and generating large data volumes requiring storage and processing

89 million **connected cars** on the road of which 6 million **self-driving** – generating and processing >1 GB of data per second each

250 million **personal health** wearables and connected pharmaceuticals for health data collection

Explosion of **(mostly unstructured) data**, growing to >40 Zetabytes from 5 Zetabytes today

…drive a reinforcing cycle of data creation, transmission, storage and processing…

Very high volumes **of low-cost semicon devices**

Massive **computing power and performance memory** in-cloud and in-vehicle

Ultrafast & **high-band-width network infrastructure**

Explosion of high-performance **storage capacity**

…driving demand for both **low-cost and high performance** semiconductor products in both memory and logic

…enabled by **the continuation of Moore's law…**

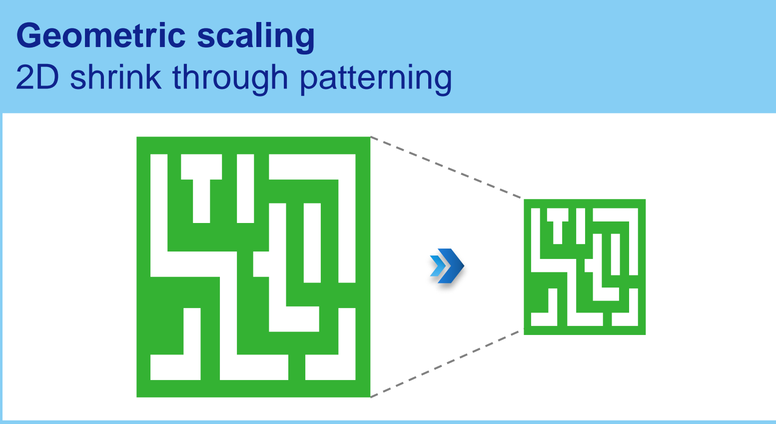
…which underpinned by an **ecosystem with combined profits of >290B$**

Source: McKinsey, ASML

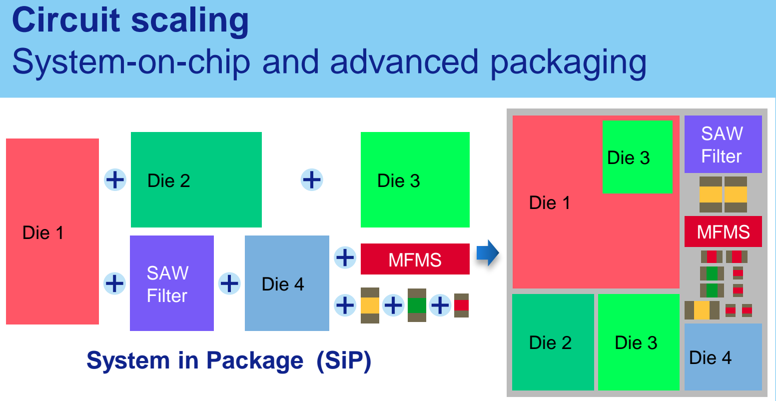
Geometrical scaling critical in support of Moore's law

now enabled trough 4 engines of innovations

Geometric scaling
2D shrink through patterning

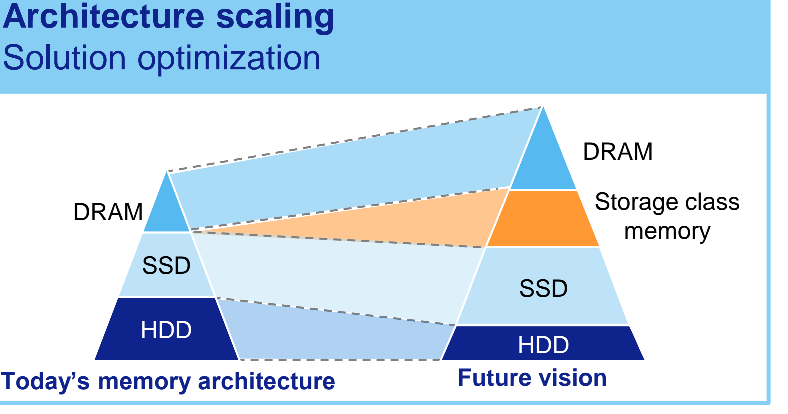


Circuit scaling
System-on-chip and advanced packaging



Device scaling
New devices and materials

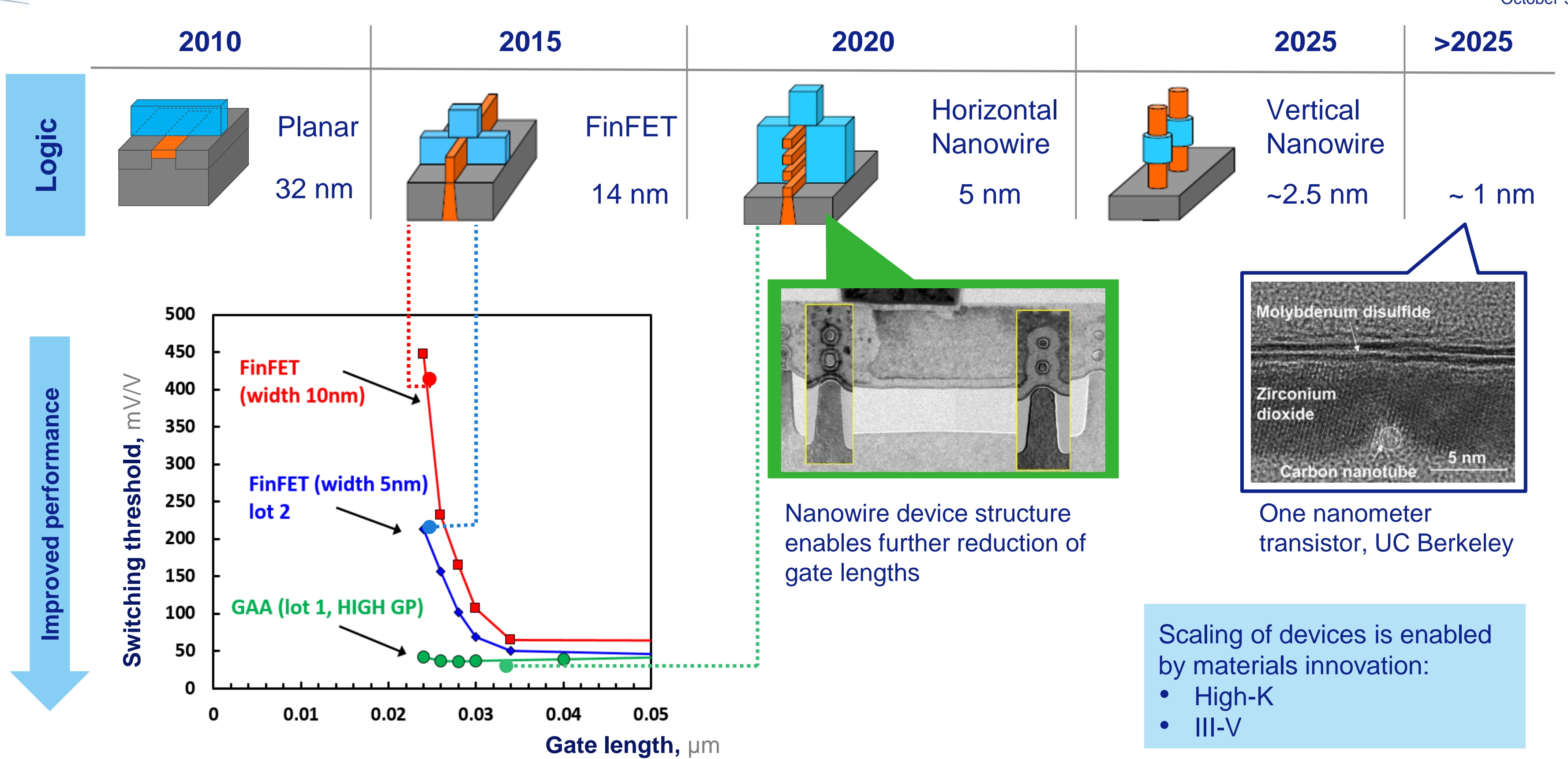
Architecture scaling
Solution optimization



Source: IMEC, customers

Logic device and shrink roadmap

New devices for 5 nm and beyond are demonstrated to work



Nanowire device structure enables further reduction of gate lengths

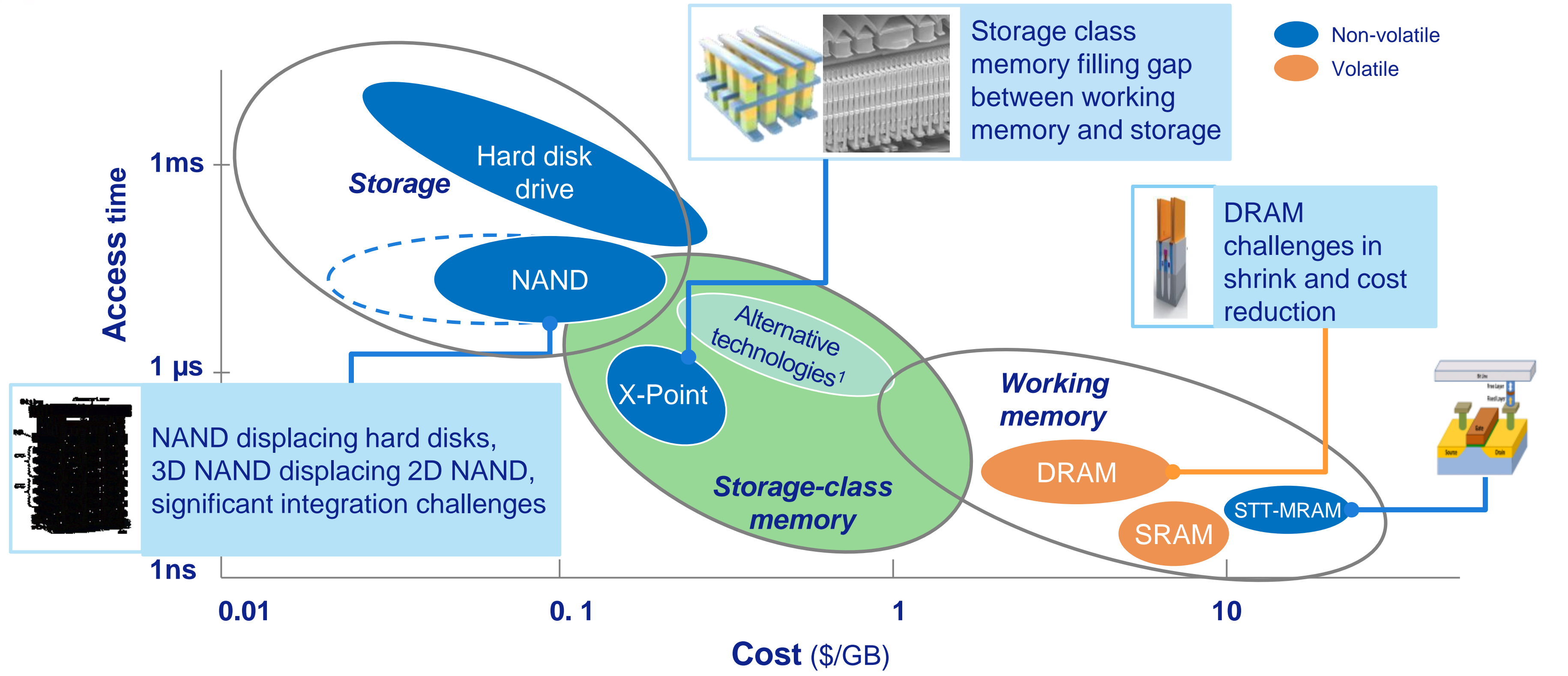
One nanometer transistor, UC Berkeley

Scaling of devices is enabled by materials innovation:

- High-K
- III-V

Source: IMEC

Large innovation ongoing in memory,
driving continued litho demand



1 Alternative technologies (e.g., CBRAM, PCRAM) likely high litho volume and performance

Source: Western Digital

Solid state replacing high performance disk memory
And new memory technologies to drive the overall performance

Relative data volume

DRAM
XPoint
SSD (NAND)
SSD (XPoint)
15K RPM HDD
10K RPM HDD
≤ 7200 RPM HDD

Source:
Micron

2015 2016 2017 2018 2019 2020

$/IOP
$/(1/µsec)

Performance metrics
- Low Latencies
- High IOPS

Memory
Semantics

StorePute

Storage
Semantics

Mobile
Automotive

Storage Servers
External Storage

$/GB
$/GBps

Performance metrics
- Bandwidth

Source: Will Akin, Micron, Short Course, IEEE IMW may 2016

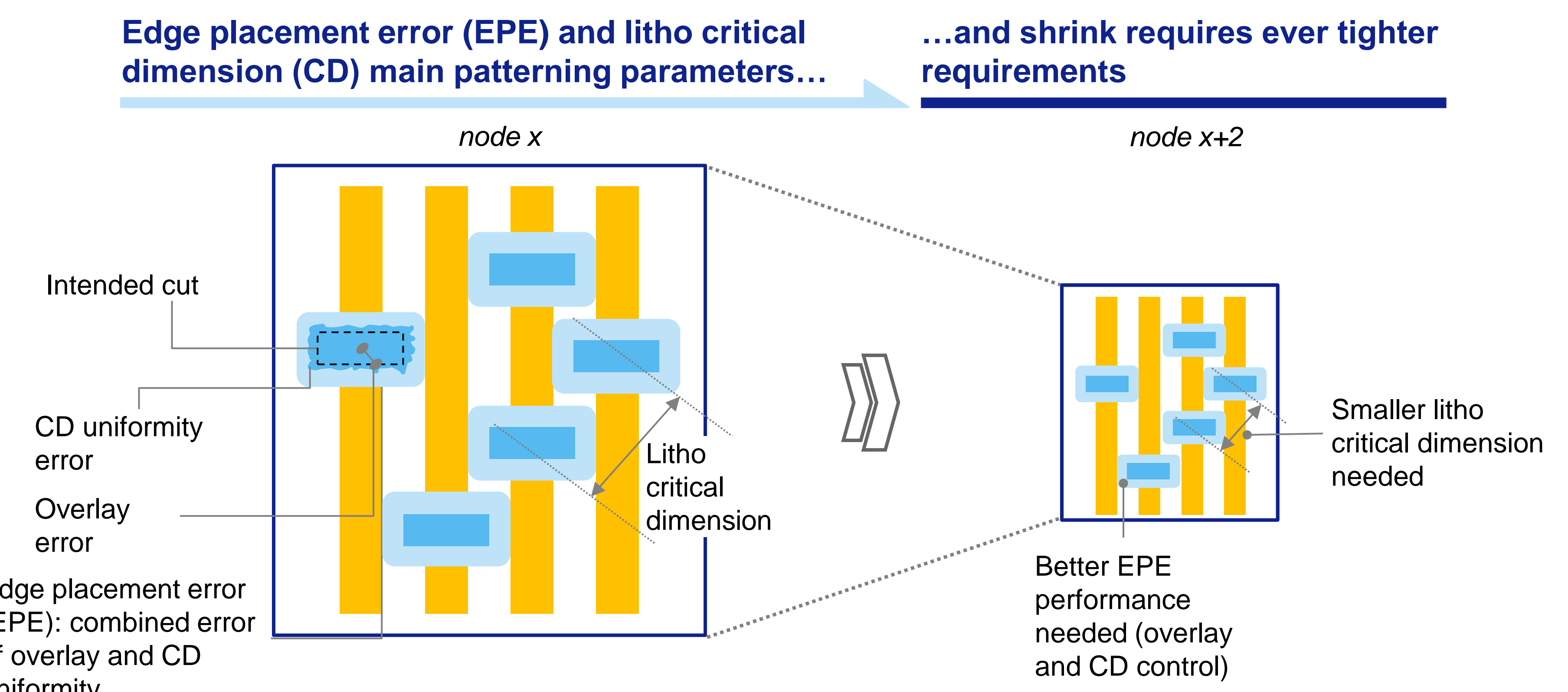
EUV could simplify customers' patterning process

	Spacer process makes 1D grids with high resolution	Litho-etch process makes 2D patterns	Final pattern
	Cross section view	*Top view*	*Top view*
Lithography	litho, hard mask	Litho step 1, Litho step 2	
Deposition	spacer deposition		
Etch		Etch step 1, Etch step 2	pitch, litho critical dimension
Resolution	Litho critical dimension / 2^n	Litho critical dimension / $\sqrt{n}$	

Note: process schematics are simplified for presentation purposes

Edge placement error & litho critical dimension challenges

are main factors for continued shrink



Single Exposure lithography is most attractive

optimizing cost, cycle time, yield and edge placement challenges

Customer perspective	Cost	Process complexity	EPE complexity
Single expose (SE)	✓	✓	-
Litho etch (LE^x)	~	~	~

Source: ASML

Industry Shrink Roadmap & EUV insertion

Public
Slide 16
October 31, 2016

EUV Production Insertion Window

HVM: 2014 | 2015 | 2016 | 2017 | 2018 | 2019 | 2020 | 2021 | 2022

Logic
20nm → 16-14nm → 10nm → 7nm → 5nm → 3nm — Node name

Performance Memory
DRAM
28-30 → 20-22 → 1X → 1Y → 1Z → next — Minimum half pitch

Storage Class Memory
PC-RAM, ReRAM, X-point etc.
2X'/x2 → 1X"/x4 → 1Y"/x8 → 1Z"/x8 — Minimum half pitch /x number of layers

Storage Memory
Planar Floating Gate NAND
22 → 17-18 → 14-15

3D NAND
x24 → x32 → x48 → x64 → >x96 → >x128 → >x192 → >x200 — x number of layers

Today's status
- Production[1]
- Development[1]
- Research[1]
- Roadmap[2]

Source: 1) Customers - public statements, IC Knowledge LLC; 2) ASML extrapolations

Strategic priorities to meet customer requirements

Grow our Litho business by delivering superior customer value

1 EUV industrialization

- Deliver high volume manufacturing performance metrics
- Enhance EUV value for future nodes

2 DUV competitiveness

- Drive **DUV performance**
  – Continue to lead in innovation
  – Drive operational excellence
  – Expand installed base business

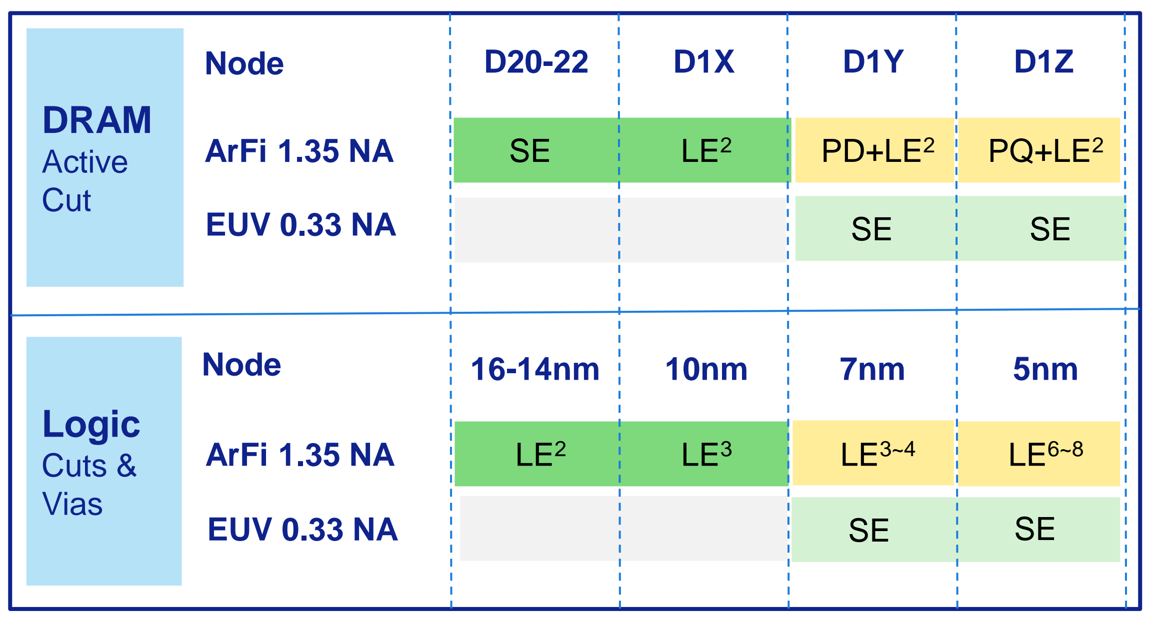
3 Holistic Litho

- Build a winning position in **Pattern Fidelity Control** leveraging inspection combined with superior computational Litho

4 EUV extension

- Deliver **High-NA EUV** in time to support customer roadmaps and avoid complex and costly alternatives

1 EUV key to drive cost effective device shrink roadmaps and simplifying immersion multiple patterning



DRAM Active Cut	D20-22	D1X	D1Y	D1Z
Node	D20-22	D1X	D1Y	D1Z
ArFi 1.35 NA	SE	LE^2	$PD+LE^2$	$PQ+LE^2$
EUV 0.33 NA			SE	SE

Logic Cuts & Vias	16-14nm	10nm	7nm	5nm
Node	16-14nm	10nm	7nm	5nm
ArFi 1.35 NA	LE^2	LE^3	$LE^{3\sim4}$	$LE^{6\sim8}$
EUV 0.33 NA			SE	SE

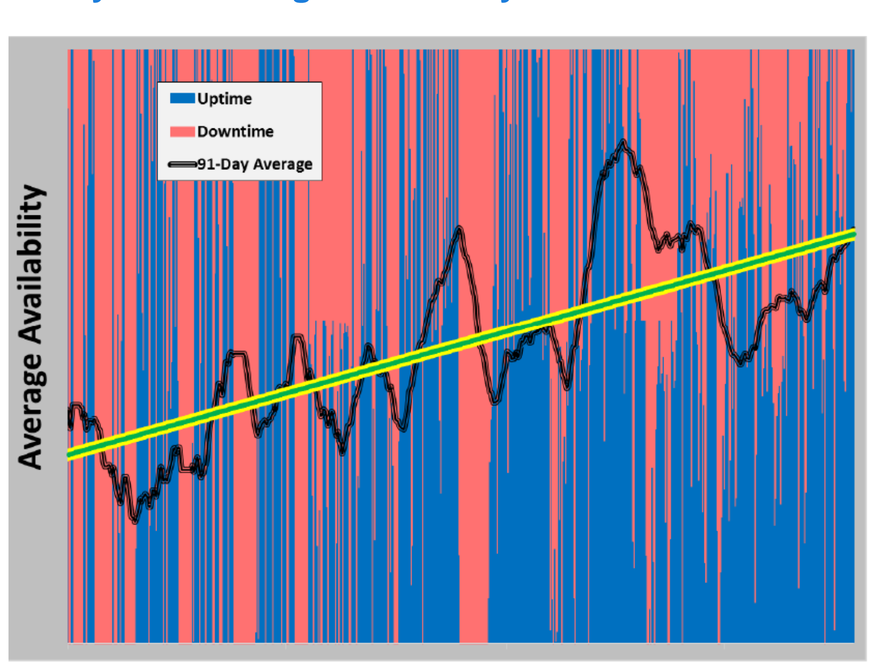
PoR, Process of Record | Plan | Possible but challenging

SE = Single Exposure, LE^n = Litho-Etch, n # repeats, PD = Pitch Doubling, PQ = Pitch Quadrupling

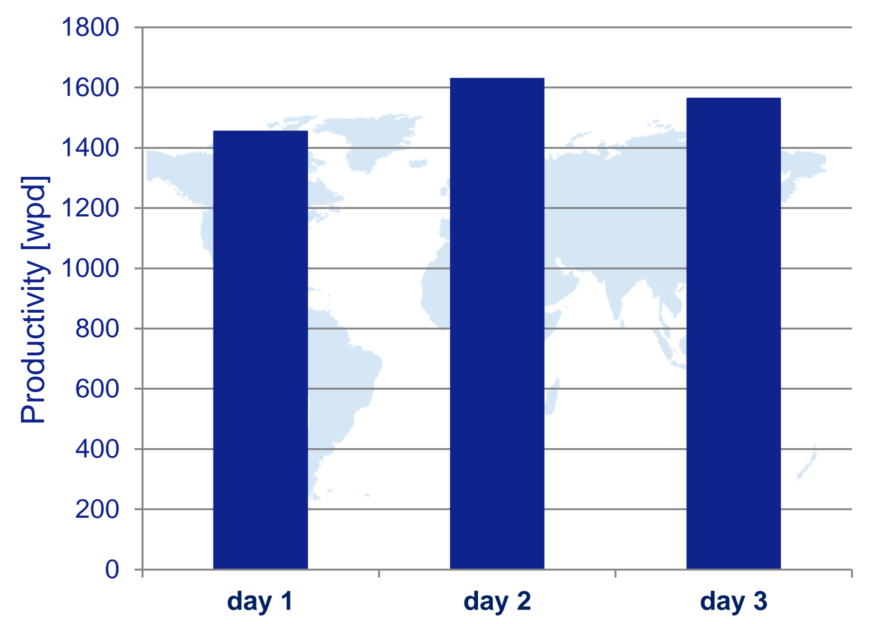
EUV industrialization: productivity and consistency

>1500 wafers per day at customer fab, variability needs improvement

System average availability at customer site



3 day average 1,500 wafer per day at customer site



Source: Britt Turkot, Intel, 2016 international symposium on EUV, 24 October 2016, Hiroshima

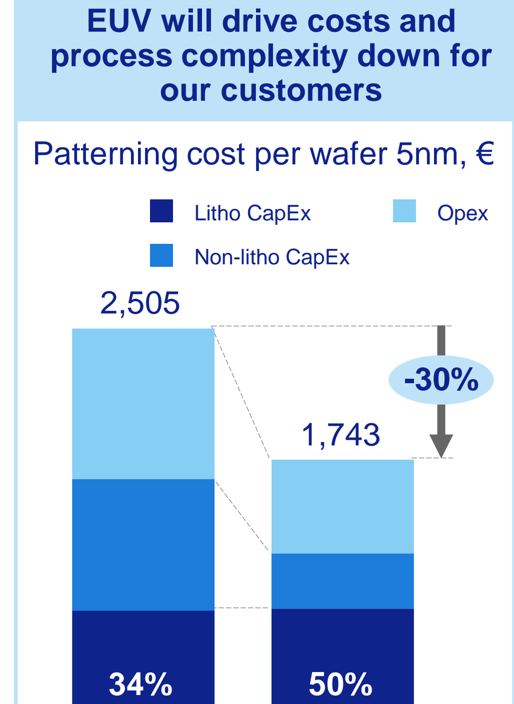
Source: TSMC, Semicon Taiwan, Sep 2016

- Source: NXE:3350B
- Each bar represents customer wafers exposed on one individual day

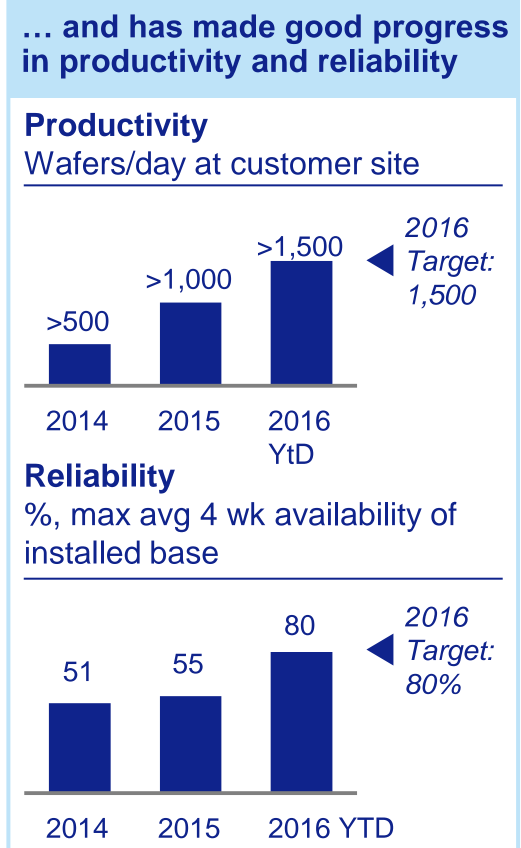
1 We will deliver continued reliability improvement

and ramp up our operations to realize EUV in volume manufacturing

EUV will drive costs and process complexity down for our customers



… and has made good progress in productivity and reliability



… triggering increased customer demand

"We plan to **extensively use EUV** in 5nm to improve density, simplify process complexity, and reduce cost…Recently EUV development gained quite a good momentum across the industry. "
Mark Liu, co-CEO TSMC, July '16

"Samsung fully intends to **deploy EUV** for 7nm, triple patterning is not viable …"
"We expect production in 2018"
AnandTech & SemiconWest '16

"Significant strides have been made … taking the technology from a question of *if* to a question of *when*. **EUV is solidly on a path to HVM insertion** as soon as the technology becomes ready and cost effective"
Intel, SPIE '16

Source: ASML, public statements

2 Drive DUV Competitiveness

DUV competitiveness…

…Our customers	…Ourselves
• Enable our **customers to execute their roadmaps cost effectively**	• Maintain our **market share** and **margins**

DUV Strategic Priorities

	NXT *(Immersion)*	**XT** *(Dry)*
Technology Leadership	**Execute roadmap of next generation products and options aligned with customer priorities**	
Operational Excellence	**Deliver high quality cost effective solutions**	

2 TWINSCAN Immersion system roadmap

introduction	190 WpH	230 WpH	250 WpH	275 WpH	>285 WpH	Overlay [nm]
2009	NXT:1950i					7
2011		NXT:196	XT:1965Ci			6
2013			NXT:			4
2015				N		3
				NXT:next1		<3
					NXT:next2	<2

At customer upgradable

products under study

Roadmap: October 2016

2

Improvements on Next Generation products

Overlay, DUV to EUV matching

Projection Lens
Optimization of lens for improved imaging and overlay

Process robust Alignment
improves overlay performance

Next slides

Process robust Leveling
Improves machine matching

Improved Grid Setup
Improved overlay and machine matching

Wafer heating control
Improved overlay performance

Wafer table
Improved machine matching

Wafer Handler
Improves overlay performance

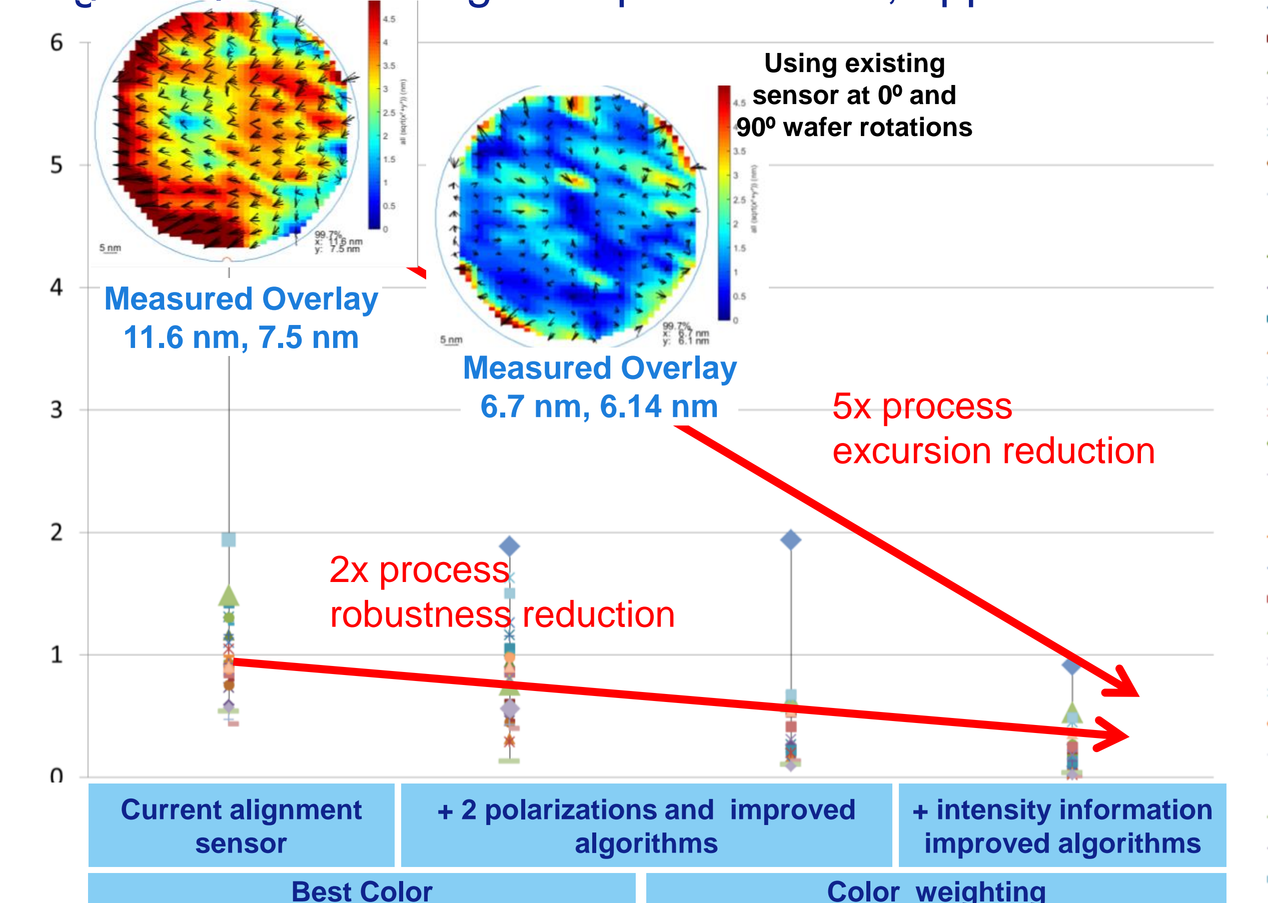
ASML
TWINSCAN NXT:1980Di
Optics by Carl Zeiss

Overlay - general

Imaging/Focus

2 Alignment process robustness improvement

Using multiple wavelengths & polarizations; applicable for DUV and EUV

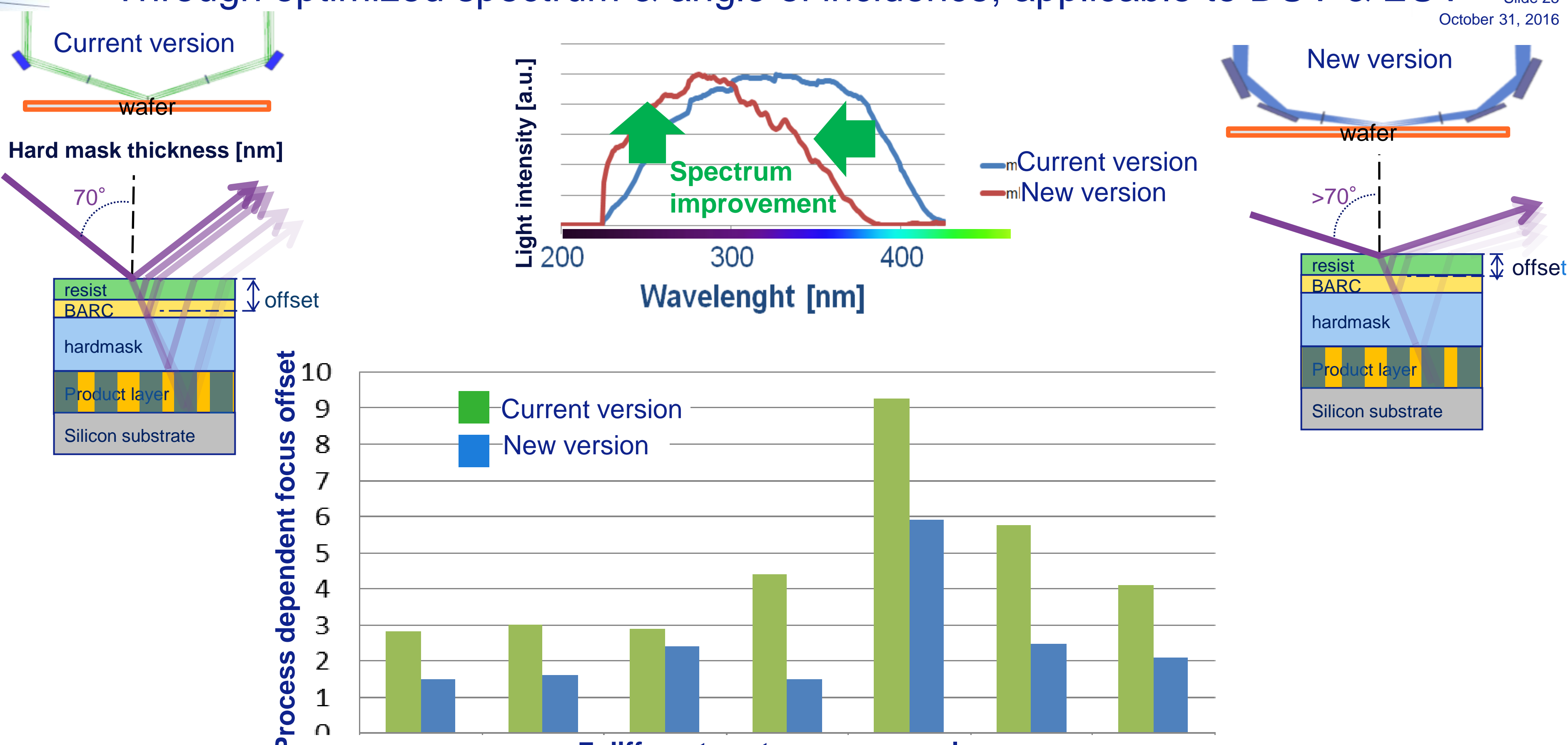


resist
BARC
carbon
ILD | copper | ILD
ILD
copper | ILD | copper
ILD
"poly"
Si wafer

30 different process stacks and marker combinations in both FEOL and BEOL

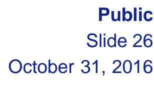
2 Improved focus and leveling process robustness

Through optimized spectrum & angle of incidence; applicable to DUV & EUV



TWINSCAN Dry system roadmap

Continued improvements in productivity and capability of all 4 product lines



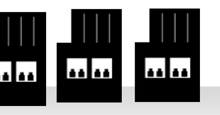
Product	Overlay	178-185	205 WpH	210 WpH	220 WpH	225 WpH	230 WpH	240 WpH
XT:400 I-line	60nm	XT:400H 365 nm		PEP	XT:400K	PEP	XT:400L	
	20nm				TOP		TOP	
XT:860 KrF	14nm	XT:860H 248 nm	PEP	XT:860K	PEP	XT:860L	PEP	XT:860M
	10nm	XT:1000H 248 nm	PEP	TOP				
XT:1000 High NA KrF	9nm	XT:1450H 193 nm	XT:1460K					
	7nm			TOP				TOP
XT:1450 ArF	6nm	TOP TOP						
	5nm		TOP XT:1060K					

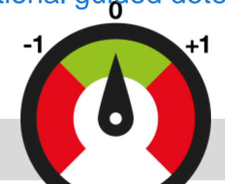
TOP — Overlay improvement
PEP — Productivity improvement

Roadmap: October 2016

3 ASML Holistic Lithography integrates 3 competences

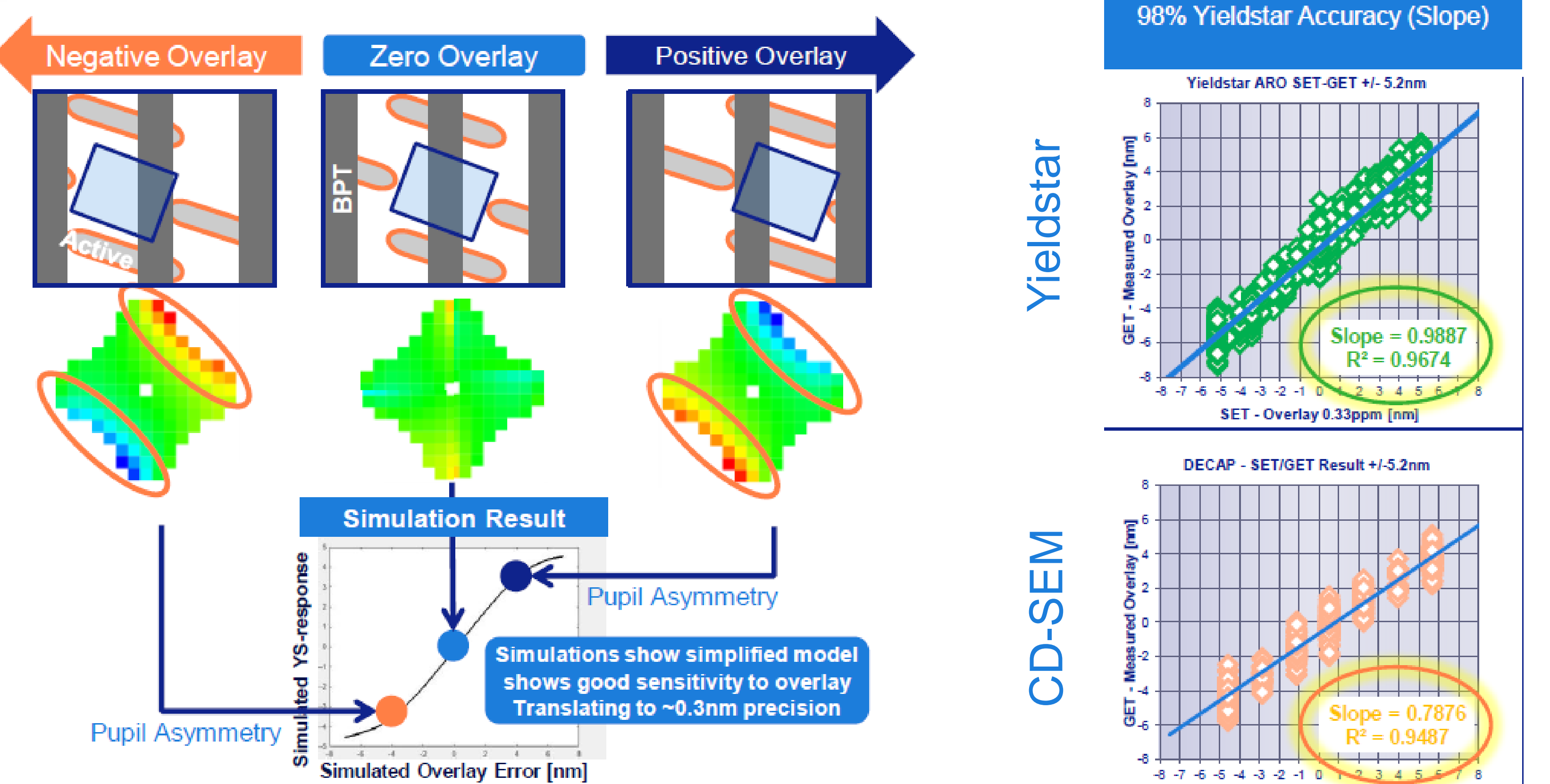
Resulting in 3 customer value propositions





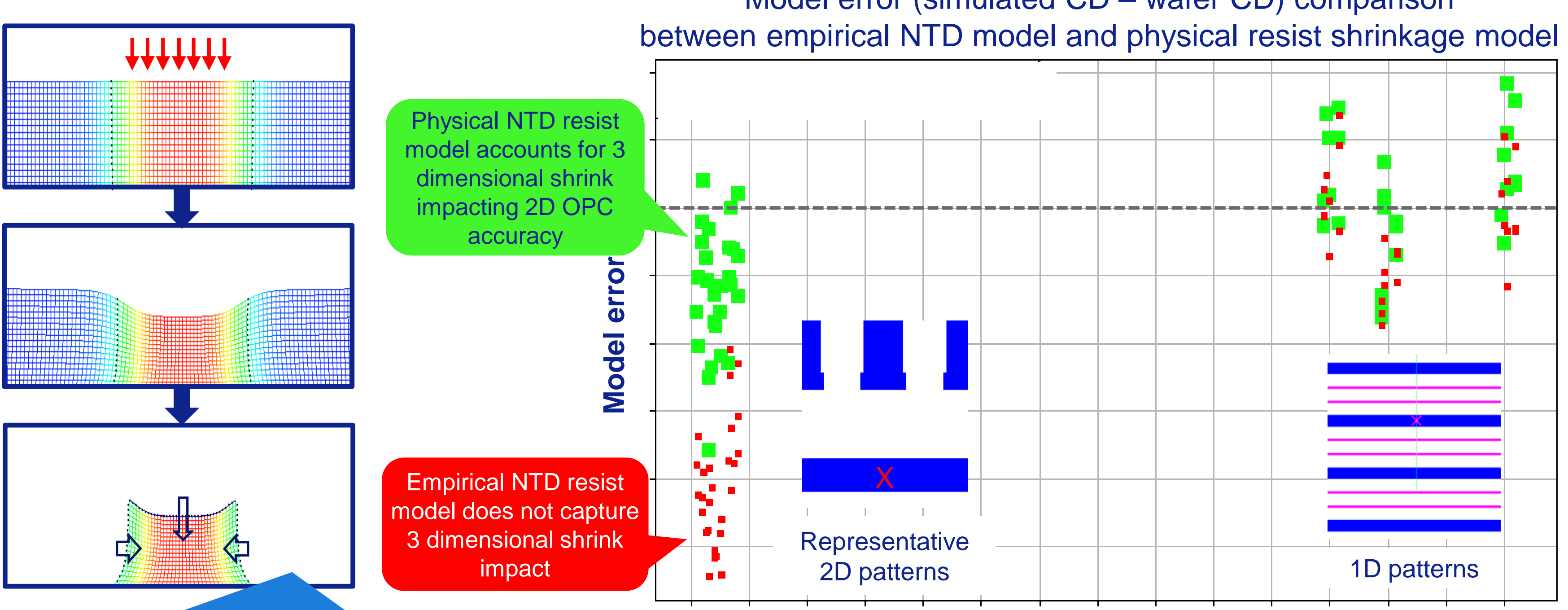
3.2 YieldStar: Unique on product overlay metrology

measuring overlay of actual device features, DRAM example

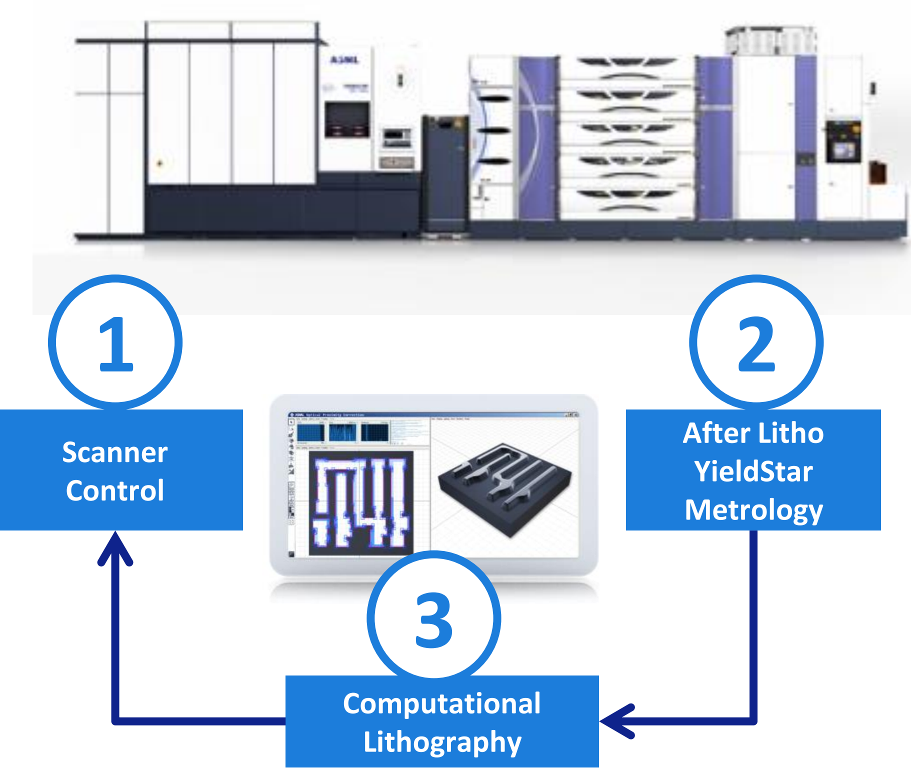


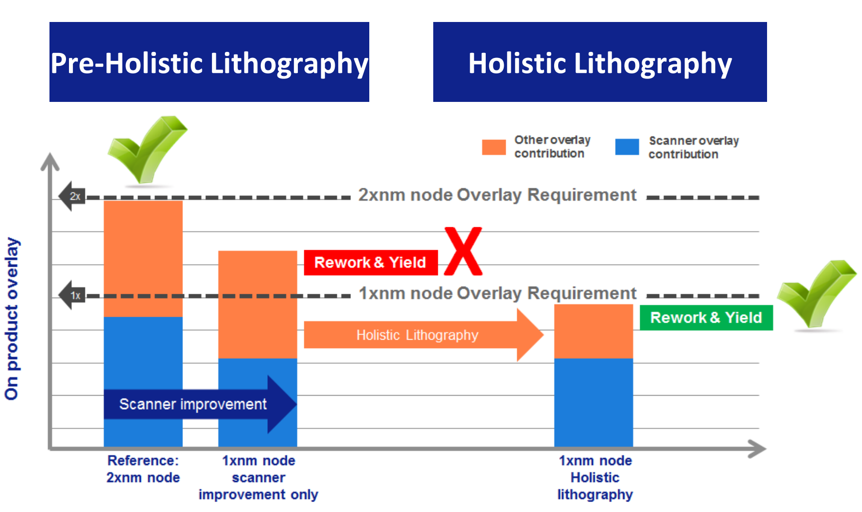
3.3 Unique Negative Tone resist modelling capability

Modelling accuracy improved 60%

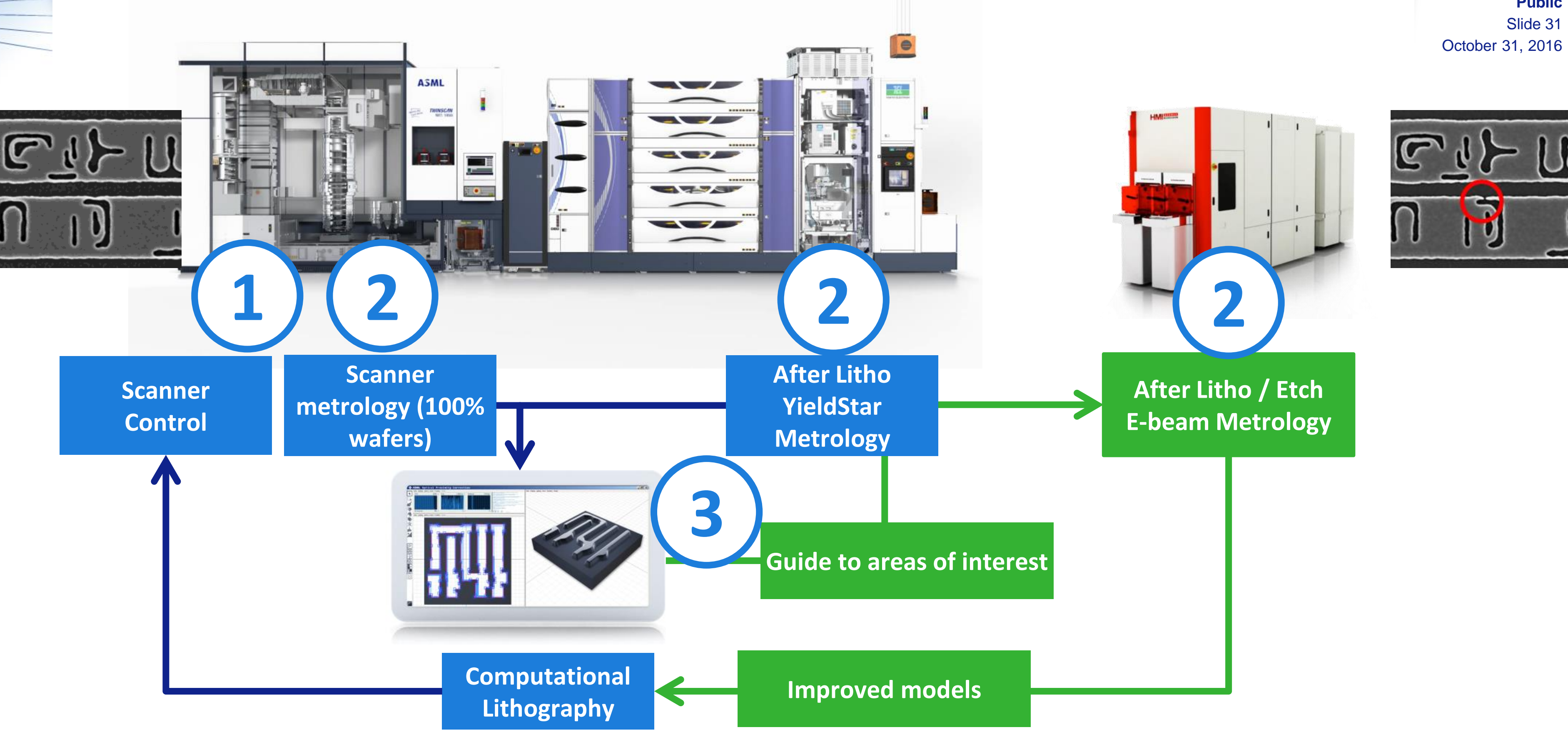


3 ASML holistic lithography at 1x nm node: Overlay Control





3 ASML holistic lithography future - Pattern fidelity control



3 ASML holistic lithography future: Pattern fidelity control: reducing pattern errors up to~ 50%

Uncontrolled
Controlled

Error count →
Hotspot count →

	HS1	HS2	HS3	HS4
Uncontrolled	26	23	36	23
Controlled	11	13	3	6
Reduction	58%	43%	92%	74%

Focus map

CD map

Pattern error prediction

Pattern error measurement

Hot spots

and reduce pattern error by ~50% by control

HMI HERMES MICROVISION

4 EUV with high-NA key to extending device shrink roadmaps and simplifying multiple patterning

	Node	D20-22	D1X	D1Y	D1Z	next
DRAM Active Cut	**ArFi 1.35 NA**	SE	LE^2	PD+LE^2	PQ+LE^2	PQ+LE^2
	EUV 0.33 NA			SE	SE	LE^2

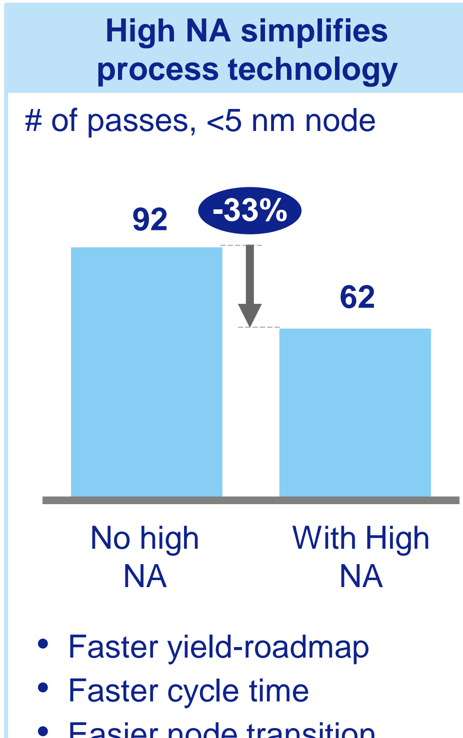
	Node	16-14nm	10nm	7nm	5nm	3nm
Logic Cuts & Vias	**ArFi 1.35 NA**	LE^2	LE^3	LE$^{3\sim4}$	LE$^{6\sim8}$	LE$^{8\sim11}$
	EUV 0.33 NA			SE	SE	LE$^{2\sim3}$
	EUV >0.5 NA				SE	SE

Legend: PoR, Process of Record (green) · Plan (light green) · Possible but challenging (yellow)

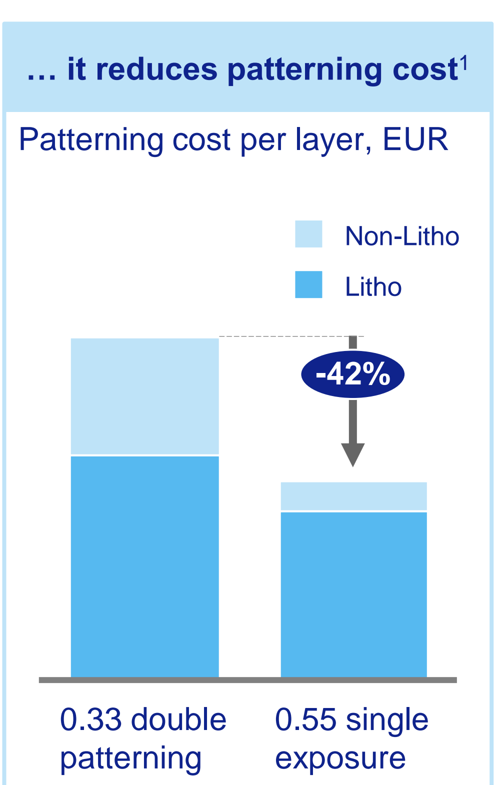
SE = Single Exposure, LE^n = Litho-Etch, n # repeats, PD = Pitch Doubling, PQ = Pitch Quadrupling

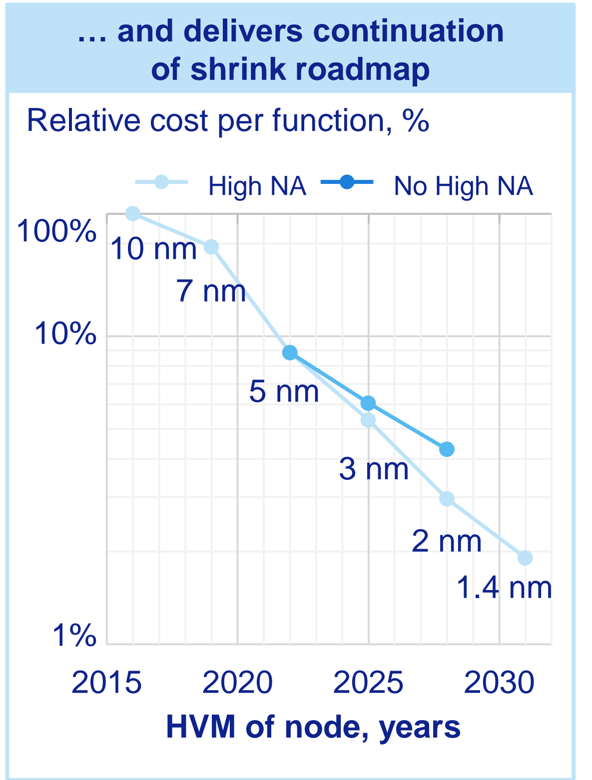
4 High NA delivers value to our customers

through process simplification, patterning cost and further shrink



- Faster yield-roadmap
- Faster cycle time
- Easier node transition



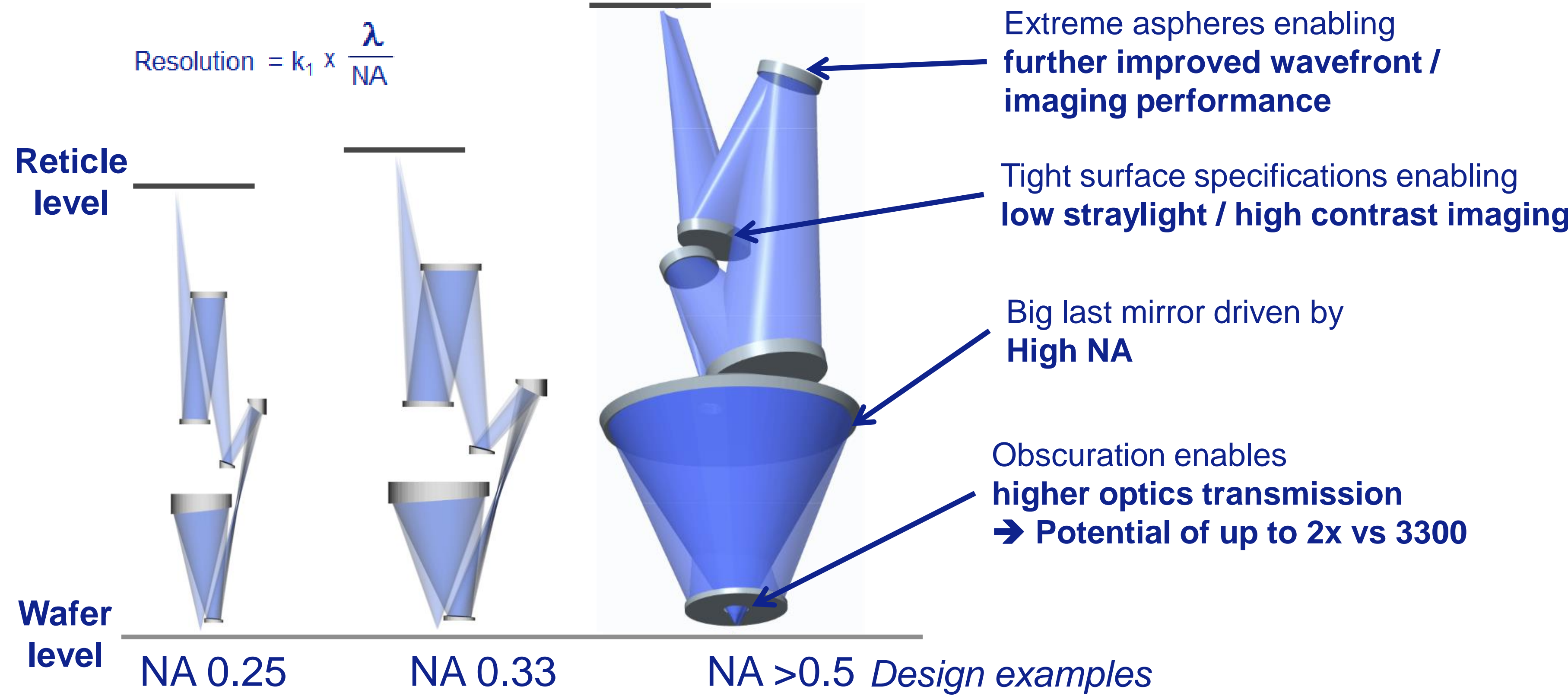


1 SE = single exposure, LE^2 = double patterning;

Source: ASML

High-NA optics design concepts available

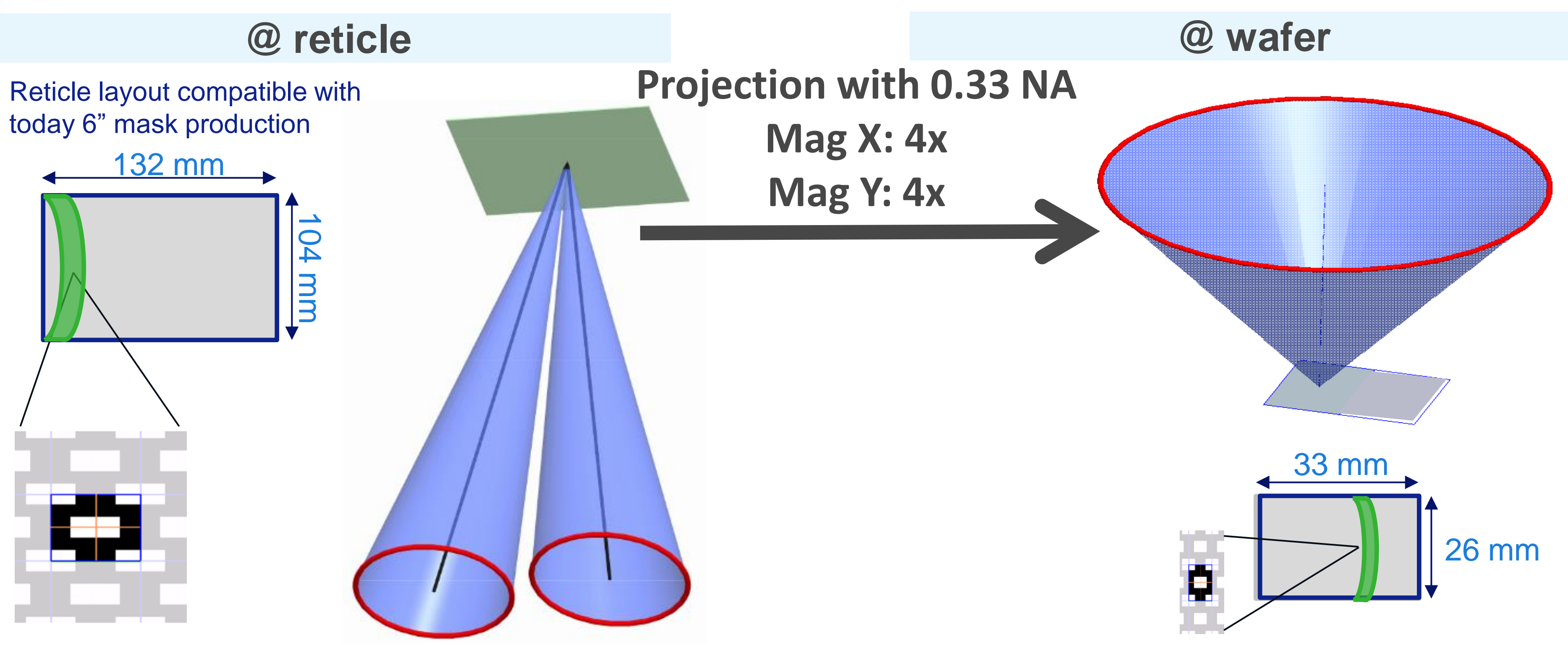
Larger elements with tighter specifications



Source: Zeiss, "EUV lithography optics for sub-9nm resolution," Proc. SPIE 9422, (2015).

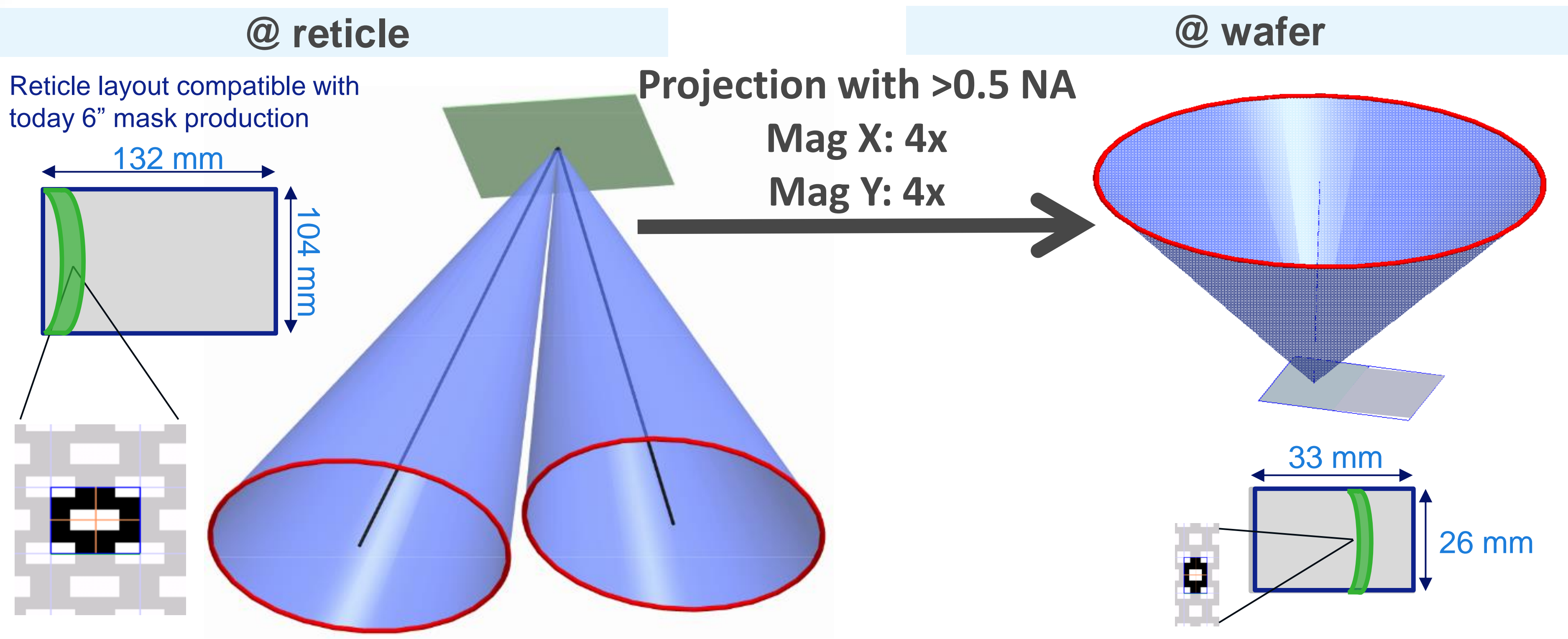
4 Anamorphic High NA EUV reduces the angles

enabling a solution with 26 mm slit on 6” masks



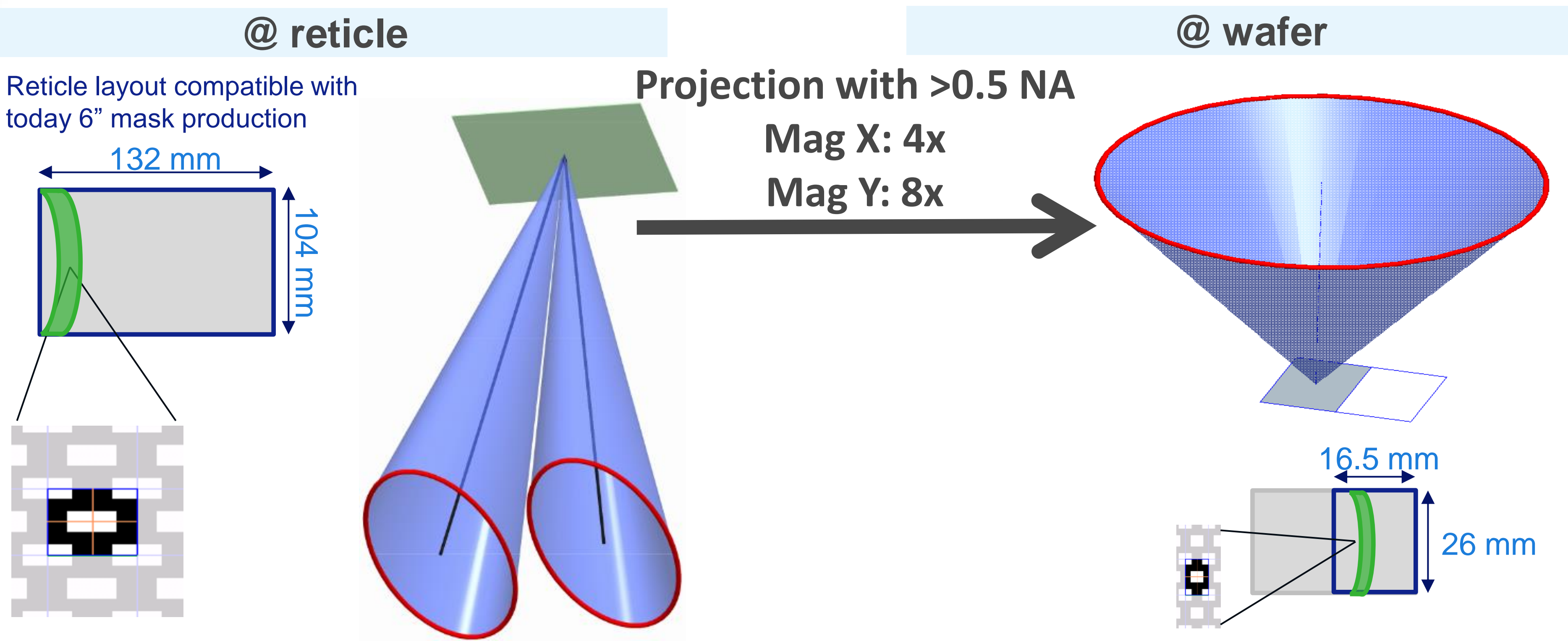
Source: Jan van Schoot, ASML, “EUV roadmap extension by higher Numerical Aperture”, 2016 international symposium on EUV, 24 October 2016, Hiroshima

4 Anamorphic High NA EUV reduces the angles
enabling a solution with 26 mm slit on 6” masks



Source: Jan van Schoot, ASML, “EUV roadmap extension by higher Numerical Aperture”, 2016 international symposium on EUV, 24 October 2016, Hiroshima

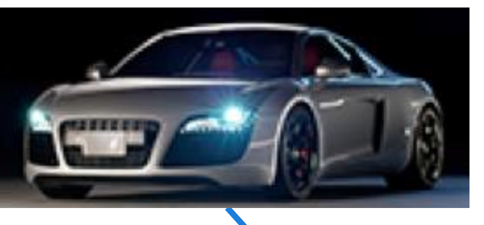
Anamorphic High NA EUV reduces the angles
enabling a solution with 26 mm slit on 6” masks



Source: Jan van Schoot, ASML, “EUV roadmap extension by higher Numerical Aperture”, 2016 international symposium on EUV, 24 October 2016, Hiroshima

4 Anamorphic optics are used in cinematography

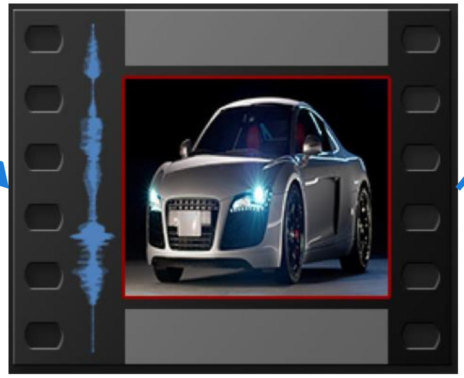
"Don't change the mask"



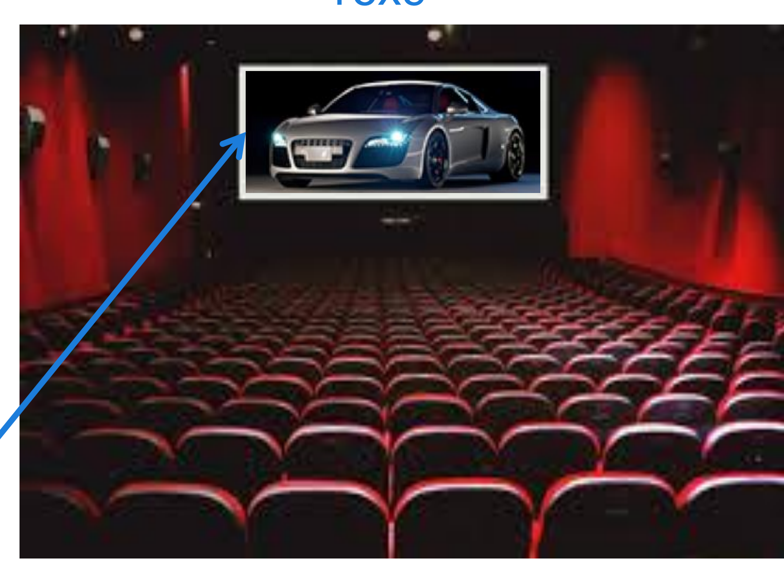
16x9

Anamorphic Lens

"The Mask"
(24x36mm^2)



16x9



Anamorphic Projector

4 High-NA delivers higher throughput

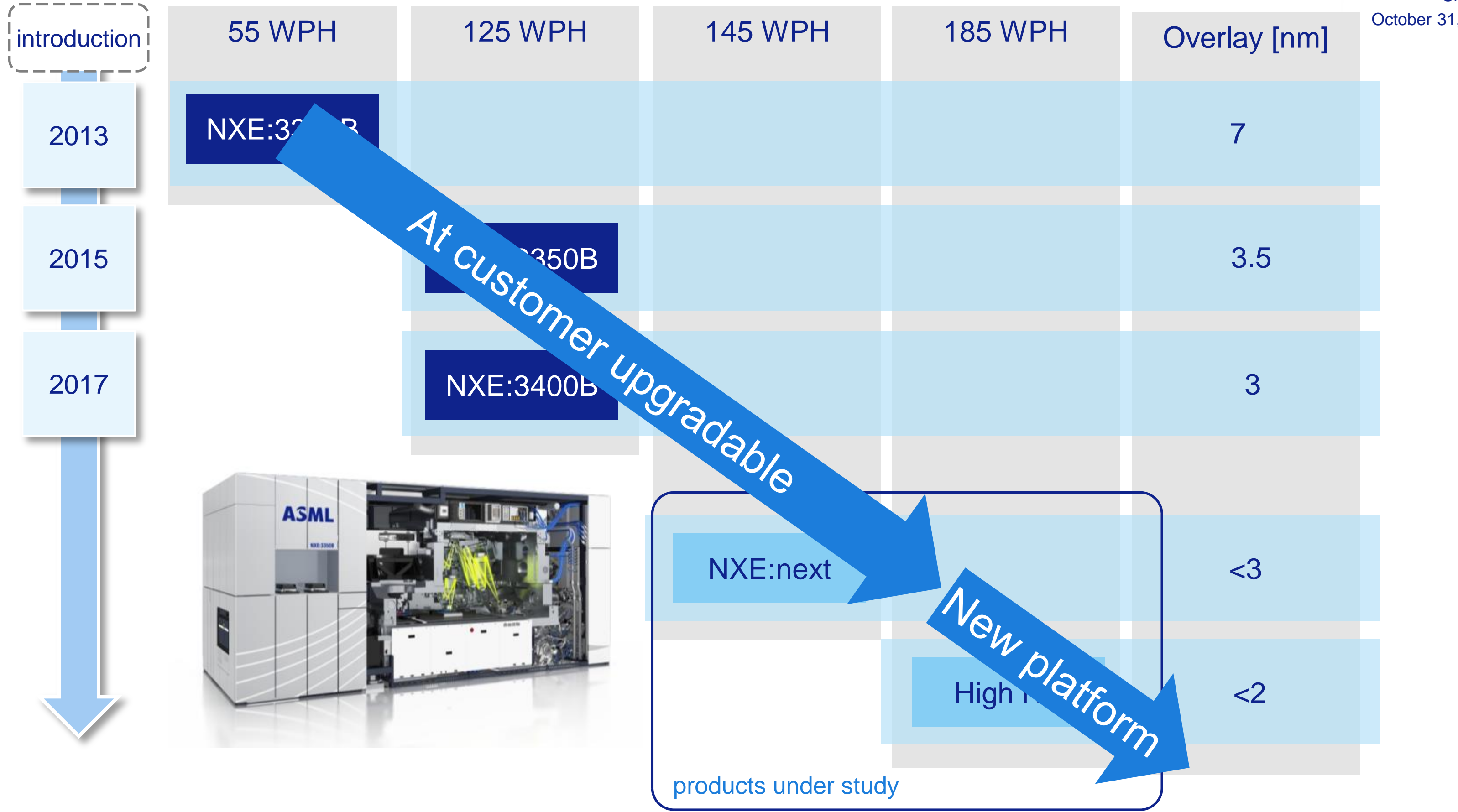
High-NA vs. 0.33NA throughput at given dose

At any power / dose, High NA delivers higher throughput than 0.33NA due to:

- Higher lens transmission
- Improved stage speeds

Source: ASML

EUV extension roadmap



Roadmap: October 2016

The future

- **Moore’s law to continue for the foreseeable future**, driven by connecting everything around us, generating massive data and enabled by geometrical device, architectural and circuit scaling. Logic device innovation and memory/computer architecture innovations in support of this.
- **EUV industrialization** enabled by identified insertion opportunity at multiple customers and execution to roadmaps progressing to plan, improvements still needed for consistency.
- **DUV competitiveness** to support continued demand given its cost advantage over EUV for less critical layers and some double patterning. Improvements in CD and overlay continued to be required for future nodes.
- **Holistic Lithography** is being extended with pattern fidelity control. Metrology extensions needed for on product robust process, after etch targets and resolution enhancements through computational enhanced e-beam capability. Increased scanner control capability to enable ultimate on product process control.
- **EUV extension** with high NA enable cost-effective shrink to continue into the next decade

Forward looking statements

ASML

This document contains statements relating to certain projections and business trends that are forward-looking, including statements with respect to our outlook, including expected customer demand in specified market segments (and underlying assumptions) including memory, logic and foundry, expected sales levels, trends, including trends towards 2020 and beyond and expected industry growth, and outlook, systems backlog, expected or indicative market opportunity, financial results and targets, including, for ASML and ASML and HMI combined, expected sales, other income, gross margin, R&D and SG&A expenses, capital expenditures, cash conversion cycle, EPS and effective annualized tax rate, annual revenue opportunity and EPS potential by end of decade and growth opportunity beyond 2020 for ASML and ASML and HMI combined, cost per function reduction and ASML system ASP, goals relating to gross cash balance and ASML's capital structure, customer, partner and industry roadmaps, productivity of our tools and systems performance, including EUV system performance (such as endurance tests), expected industry trends and expected trends in the business environment, the addition of value through delivery of lithography products and the achievement of cost-effective shrink, expected continued lithography demand and increasing lithography spend, the main drivers of lithography systems, lithography intensity for all market segments, customer execution of shrink roadmaps, future memory application distribution, expected addressable markets, including the market for lithography systems and service and options, expected manufacturing and process R&D, statements with respect to growing end markets that require fab capacity driving demand for ASML's tools, statements with respect to the acquisition of HMI by ASML, including market opportunity, the expected timing of completion of the HMI acquisition and delisting of HMI, the expected benefits of the acquisition of HMI by ASML, including expected continuation of year on year growth, the provision of e-beam metrology capability and its effect on holistic lithography solutions, including the introduction of a new class of pattern fidelity control and the improvement of customers' control strategy, statements with respect to EUV, including targets, such as availability, productivity, facilities and shipments, including the number of EUV systems expected to be shipped and timing of shipments, and roadmaps, shrink being key driver to industry growth, expected industry adoption of EUV and statements with respect to plans of customers to insert EUV into production and timing, the benefits of EUV, including expected cost reduction and cost-effective shrink, the expected continuation of Moore's law, without slowing down, and that EUV will continue to enable Moore's law and drive long term value, goals for holistic lithography, including pattern fidelity control, expectations relating to double patterning, immersion and dry systems, intention to return excess cash to shareholders, statements about our proposed dividend, dividend policy and intention to repurchase shares and statements with respect to the current share repurchase plan. You can generally identify these statements by the use of words like "may", "will", "could", "should", "project", "believe", "anticipate", "expect", "plan", "estimate", "forecast", "potential", "intend", "continue" and variations of these words or comparable words. These statements are not historical facts, but rather are based on current expectations, estimates, assumptions and projections about the business and our future financial results and readers should not place undue reliance on them.

Forward-looking statements do not guarantee future performance and involve risks and uncertainties. These risks and uncertainties include, without limitation, economic conditions, product demand and semiconductor equipment industry capacity, worldwide demand and manufacturing capacity utilization for semiconductors (the principal product of our customer base), including the impact of general economic conditions on consumer confidence and demand for our customers' products, competitive products and pricing, the impact of any manufacturing efficiencies and capacity constraints, performance of our systems, the continuing success of technology advances and the related pace of new product development and customer acceptance of new products including EUV, the number and timing of EUV systems expected to be shipped and recognized in revenue, delays in EUV systems production and development, our ability to enforce patents and protect intellectual property rights, the risk of intellectual property litigation, availability of raw materials and critical manufacturing equipment, trade environment, changes in exchange rates, changes in tax rates, available cash and liquidity, our ability to refinance our indebtedness, distributable reserves for dividend payments and share repurchases and timing of resumption of the share repurchase plan, and other risks indicated in the risk factors included in ASML's Annual Report on Form 20-F and other filings with the US Securities and Exchange Commission. These forward-looking statements are made only as of the date of this document. We do not undertake to update or revise the forward-looking statements, whether as a result of new information, future events or otherwise.

INVESTOR DAY

ASML SMALL TALK 2016

NEW YORK CITY