The Applications business is projected to grow at ~20% CAGR with strong gross margins over the period 2020 through 2025.

The Applications product portfolio supports the ASML scanner business, driven by our unique capability to help customers maximize patterning performance:

- Driving improvements in Edge Placement Error (EPE)
- Delivering leading solutions for optical and e-beam metrology and inspection
- Integrating ASML’s complete product portfolio into a Holistic Litho solution to optimize and control the litho process

Primary drivers of growth are the extension of our EPE roadmap:

- New metrology, inspection and control offerings extend the roadmap
- Innovative products combine computational technology, YieldStar overlay metrology and e-beam metrology
- Hardware and software products support the introduction of EUV into HVM
- New applications of deep learning in both computational litho and defect inspection drive improved performance
• Markets and product roadmap
Holistic lithography
Driving improvements in EPE
E-beam inspection
Growth opportunities in Applications arise from technology shifts in key market segments

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<th>Industry driver</th>
<th>Technology shifts</th>
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<td>Resolution</td>
<td>Single Beam / Optical → Multibeam</td>
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<td>Throughput</td>
<td>Optical Overlay: Image-based to diffraction-based</td>
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<td>Parts per billion failure measurements</td>
<td>Optical Overlay: Targets → Device</td>
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<td>Accuracy</td>
<td>E-beam: Small field → Large field</td>
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<td>Precision</td>
<td>Physical models → Deep learning</td>
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<td>Massive metrology</td>
<td>Rectangular → Freeform mask patterns</td>
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<td>Model accuracy</td>
<td>CPU → Hybrid/GPU compute</td>
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<td>Compute cost</td>
<td>Overlay / CD → EPE</td>
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<td>Transition to EPE</td>
<td>HVM: DUV → DUV + EUV</td>
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<td>EUV to HVM</td>
<td>Low → Higher order scanner corrections</td>
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<td>Advanced corrections</td>
<td>2017 €3.3B</td>
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<td>2020 €4.0B</td>
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<td>2025 €6.7B</td>
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TAM based on ASML interpretation of VLSI Research and Gartner
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<tr>
<th>Category</th>
<th>2020</th>
<th>2021</th>
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<td><strong>Scanner Interfaces and Control Software</strong></td>
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<td>Fast Stages, Multiple Wavelengths, Computational Metrology, In-Device Metrology</td>
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<td><strong>Computational Lithography</strong></td>
<td>Improved Model Accuracy, Inverse OPC, Machine and Deep Learning, Etch Models</td>
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Markets and product roadmap
• Holistic lithography
Driving improvements in EPE
E-beam inspection
Our holistic portfolio is more important than ever

Lithography scanner with advanced control capability

Process window
Prediction and Enhancement

Overlay/Focus

Overlay CD

Process window
Control

Optical proximity correction

Computational lithography and computational metrology

Process window
Detection

Optical metrology
E-beam metrology
E-beam inspection
Our holistic portfolio is more important than ever

Lithography scanner with advanced control capability

Process window
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Optical metrology
E-beam metrology
E-beam inspection

Process window
Control

EUV: NXE and EXE platforms

DUV: XT and NXT platforms

Etch and deposition tools

E-beam metrology

YieldStar

E-beam

EUV: NXE and EXE platforms

DUV: XT and NXT platforms

Etch and deposition tools
Our holistic portfolio is more important than ever
All data available at every step in the flow

Use scanner metrology, YieldStar, HMI metrology and inspection to optimize sampling for scanner control, and as yield proxy for faster time-to-yield

Virtual Computing Platform

VCP

ASML

Customer
Markets and product roadmap
Holistic lithography
• Driving improvements in EPE
E-beam inspection
Reducing Edge Placement Error (EPE) is key to improve yield
Local CD errors, due to stochastics, become increasingly important

Edge Placement Error (EPE): combined error of overlay and CD uniformity (global CDU, local CD errors and OPC error)

EPE is the best predictor of yield
YieldStar overlay metrology – after litho and after etch
Characterizing the process error and enabling accurate feature placement

Litho overlay control: after Litho sparse + after Etch refine

Optical overlay metrology – after Litho

Accurate overlay on targets

YS385

Metrology data

~800 Points x 4 wafers
Every lot

Optical overlay metrology – after Etch

Accurate overlay on actual device

YS1385

Metrology data

~10,000 Points x 2 wafers
Every few days

Corrections

Litho

Etch
Driving improvements in EPE
Requires high fidelity, fast and accurate metrology to maximize the scanner’s correction capabilities

- Pattern as designed
- YieldStar
- HMI ePx
- Wafer Signature

**Metrology**
- Overlay
  - Layer B to Layer A
- Single layer EPE
  - Layer A
  - Layer B
- Single layer EPE
  - >10 million measurements/wafer 60 min

**Monitoring**
- Final Dual Layer EPE
- Computational EPE Control Software

**Control**
- Die Yield (Dies in spec)
  - Increased Yield
  - OVL and CD corrections, independently
  - EPE-aware corrections

>1,000 measurements/wafer <5 mins
>10 million measurements/wafer 60 min
>10 million measurements/wafer 60 min
ASML scanners to improve EPE and yield

ASML scanners are uniquely able to find, measure and correct for patterning variations

FlexRay illuminator

Dose manipulator

Reticle stage

Metrology stage

Exposure stage

Wafer stage

100% of wafers are measured

100% of wafers are processed field-by-field

Scanner actuators correct on a field-by-field basis

Increase in Scanner Correction Parameters per Wafer Lot (1980-2020)

...to 100,000 per lot

From <10 per lot...
Tighter EPE requirements drive increased metrology
ASML provides accurate, cost-effective overlay, EPE, and defect metrology

Measurements per lot

- Overlay
- EPE
- Defects

EPE Requirement

2015 2018 2021 2024 2027 2030
EPE requirement [nm]

Overlay
EPE
Defect Inspection
Need for part per billion control strategy
Defect-aware monitoring and control in the age of EUV stochastics

Today, server chips can be \(~800\text{mm}^2\) in size
Need for part per billion control strategy
Defect-aware monitoring and control in the age of EUV stochastics

There can be >100M contact holes per mm$^2$ and increasing by 1.5x per node

Today, server chips can be ~800mm$^2$ in size
Need for part per billion control strategy
Defect-aware monitoring and control in the age of EUV stochastics

so ~80B of these need to function

There can be >100M contact holes per mm\(^2\) and increasing by 1.5x per node

Today, server chips can be ~800mm\(^2\) in size
Markets and product roadmap
Holistic lithography
Driving EPE improvements
• E-beam inspection
High resolution E-beam versus Optical bright field inspection

High resolution e-beam provides superior resolution to optical inspection, enabling detection of tiny pattern fidelity defects.

- Customer design scaling down to 10nm feature size
- Optical bright field inspection lacks sensitivity
- E-beam capable of capturing part per billion pattern fidelity defects with nanometer resolution
E-beam inspection has inherent resolution advantage

Increasing throughput through increasing parallelism with multibeam

Defect size [nm]

Throughput [mm²/hr]

Optical Bright Field Inspection

Gen 3 Multibeam (~2028)

Gen 2 Multibeam (~2024)

Gen 1 Multibeam (2021)

Single e-beam (R&D)

Min defect size for 2 nm node and below

Increased throughput enables additional HVM applications

Scanning electron microscope image

Public
E-beam inspection: Voltage Contrast (VC) and physical defect
Unique capability of electron beam inspection to find yield limiting defects

VC inspection: detection of interlayer defects causing electric opens and shorts

- Heavily used in DRAM and 3D NAND

Physical inspection: detection of intralayer defects such as design and process weak spots

- Used in all market segments

- HMI is the technology leader in e-beam inspection
- HMI leadership enabled by high current, charging control, and fast data rates
Multibeam addresses both VC and physical defect inspection
Delivering cost-effective throughput gains at high resolution

VC inspection: detection of interlayer defects causing electric opens and shorts

Physical inspection: detection of intralayer defects such as design and process weak spots
Multibeam leverages ASML core technologies
Increasing e-beam inspection throughput for high-volume manufacturing

1. HMI’s Advanced Electron Optics & MEMS
   - High quality SEM images
   - with 9 beams scanning simultaneously

2. ASML’s stage technology:
   - High speed motion
   - High position accuracy

3. Brion’s computational technology:
   - Deep-learning-enabled image quality enhancement
   - Design-based defect inspection

Multibeam systems now shipped and installed at customers
Multibeam: current status
Implementing learnings from eScan1000 (3x3) and driving eScan1100 (5x5) qualification for first shipment expected in Q4 2021

Key messages
- Multibeam technology is challenging
- We experienced some program delays: ended original development partnership, COVID
- We added additional expertise to the team and developed new multibeam IP
- We remain confident about multibeam and are committed to realizing its market potential

Status today
- 3 eScan1000 prototypes (3x3 beams) running and under assessment at customers
- System qualification of eScan1100 (5x5 beams) moving full speed; first shipment expected Q4 2021
Applications products and business opportunity

Key messages

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Forward Looking Statements

This presentation contains statements that are forward-looking, including statements with respect to expected industry and business environment trends including expected growth, outlook and expected financial results, including expected net sales, gross margin, R&D costs, SG&A costs and effective tax rate, annual revenue opportunity for 2025, financial model for 2025 and assumptions and expected growth rates and drivers, expected growth including growth rates 2020-2025 and 2020-2030, total addressable market, growth opportunities beyond 2025 and expected annual growth rate in lithography and metrology and inspection systems and expected annual growth rate in installed base management, expected trends in addressable market up to 2030, expected trends in Logic and Memory revenue opportunities, long term growth opportunities and outlook, expected trends in demand and demand drivers, expected benefits and performance of systems and applications, semiconductor end market trends, expected growth in the semiconductor industry including expected demand growth and capital spend in the coming years, expected wafer demand growth and investments in wafer capacity, expected lithography market demand and growth and spend, growth opportunities and drivers, expected trends in EUV and DUV demand, sales, outlook, roadmaps, opportunities and capacity growth and expected EUV adoption, profitability, availability, productivity and output and estimated wafer demand and improvement in value, expected trends in the applications business, expected trends in installed base management including expected revenues and target margins, expected trends and growth opportunity in the applications business, expectations with respect to high-NA, the expectation of increased output capacity, plans, strategies and strategic priorities and direction, expectation to increase capacity, output and production to meet demand, the expectation that Moore's law will continue and Moore's law evolution, product, technology and customer roadmaps, and statements and intentions with respect to changes in exchange and tax rates, available liquidity and distributable reserves for, and other factors impacting, dividend payments and share repurchases, results of the share repurchase programs and other risks indicated in the risk factors included in ASML's Annual Report on Form 20-F for the year ended December 31, 2020 and other filings with and submissions to the US Securities and Exchange Commission. These forward-looking statements are made only as of the date of this document. We undertake no obligation to update any forward-looking statements after the date of this report or to confirm such statements to actual results or revised expectations, except as required by law.